UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FREDERICK S. DUNLAP and JOHN EITRHEIM

Appeal 2007-0452
Application 09/477,099
Technology Center 2100

Decided: June 19, 2007

Before JAMES D. THOMAS, JOHN C. MARTIN, and
JOSEPH F. RUGGIERO, *Administrative Patent Judges.*

MARTIN, *Administrative Patent Judge.*

DECISION ON APPEAL

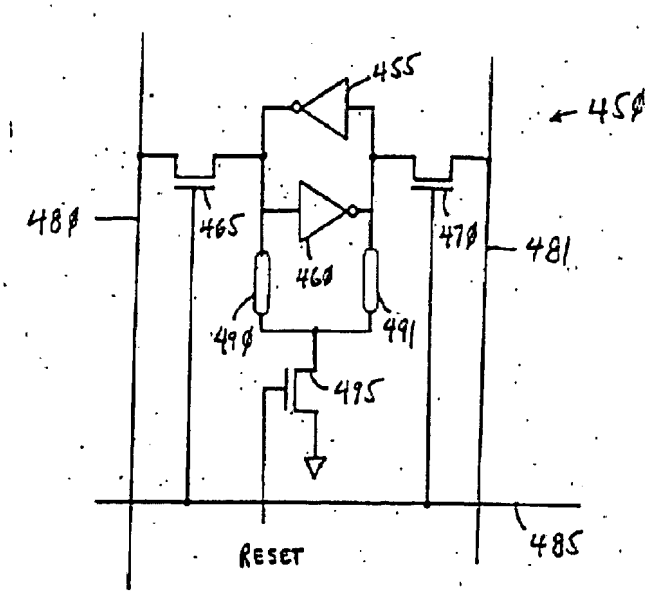
This is an appeal from the Examiner's Final Office Action rejecting claims 1-9 and 11-19 under 35 U.S.C. § 102(b) and claims 10 and 20 under 35 U.S.C. § 103(a). In view of Appellants' statement that only the rejection of claims 10 and 20 is being appealed (Br. 2), the appeal is hereby dismissed with respect to claims 1-9 and 11-19. No claims stand allowed.

We have jurisdiction under 35 U.S.C. §§ 6(b) and 134(a). We reverse.

APPELLANTS' INVENTION

Appellants' invention is an SRAM having cells that can be individually programmed to selected states in response to a power reset and thereby initially represent an embedded boot-up program (Specification 3:3-10). After the boot-up program has been executed, the microprocessor can reuse those memory cells as a cache area or as dedicated on-chip memory (*id.* at 2:4-7). For example, the memory cells can initially store an encryption program or decryption codes that can be erased before the SRAM is accessed by other software programs (*id.* at 5:18-22).

Figures 2 and 3 show two different embodiments. The rejected claims are directed to the embodiment of Figure 3, reproduced below:



The SRAM cell includes a latch formed by inverters 455 and 460 (*id.* at 18:18-20). Numerals 490 and 491 are programmable connects (*id.* at 17:19) that are connected to the drain of a transistor 495 having its source connected to ground.[1] Transistor 495 is responsive to a reset signal that goes positive (logic 1) for a short time after power is applied (*id.* at 18:8-11; 19:13-15). If the connect 491 has been removed and connect 490 remains, the input of inverter 460, which is coupled to the output of inverter 455, is pulled to ground (logic 0), causing the output of inverter 460 (which is the output of the latch) to go to logic 1 (*id.* at 18:11-20). If, on the other hand, connect 490 was removed and connect 491 remains, the output of inverter 460 (the output of the latch) is forced to logic 0 (*id.* at 18:21 to 19:2).

THE CLAIMS

Claims 1 and 10 read as follows:

1. A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:

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[1] At page 17, lines 16-19, the Specification incorrectly describes the drain as connected to ground and the source as connected to the programmable connects. However, the Specification elsewhere correctly describes the transistor as being used to short the drain to ground (e.g., *id.* at 18:9-11).

> a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and
>
> a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and
>
> a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program.

10. The SRAM device as set forth in Claim 1 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

The Brief incorrectly reads the first and second I/O lines recited in claim 1 on column lines 480 and 481 and row line 485 in the Figure 3 embodiment (Br. 3:1-2). Claim 1 calls for using the recited biasing circuit to force the first and second I/O lines to a known logic state. In Figure 3, it is the outputs of the inverters that are forced into known logic states, not the column and row lines. The recited first and second I/O lines therefore read on lines directly connected to the outputs of the inverters.

THE REFERENCES AND REJECTION

The references relied on by the Examiner are:

Shimazu	US 4,777,623	Oct. 11, 1988
Matsumura	US 5,365,475	Nov. 15, 1994

Claims 10 and 20 stand rejected under 35 U.S.C. § 103(a) for obviousness over Matsumura in view of Shimazu.

THE ISSUE

Has the Examiner made out a prima facie case for the obviousness of the subject matter of claims 10 and 20?

PRINCIPLES OF LAW

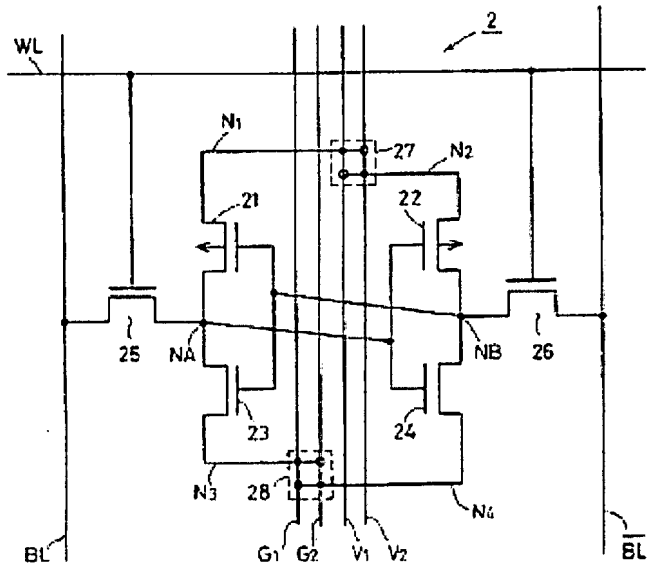
"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). A rejection under 35 U.S.C. § 103(a) must be based on the factual determinations required by the, namely, (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness. *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1360, 80 USPQ2d 1641, 1645 (Fed. Cir. 2006) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)). Where the claimed subject matter involves more than the simple substitution one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, "there

must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)). Such reasoning can be based on interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR*, 127 S. Ct. at 1740-41, 82 USPQ2d at 1396.

DISCUSSION

Matsumura discloses various embodiments of SRAMs having cells that can be individually programmed to function either as a RAM cell or a ROM cell. The Examiner relies on the embodiment depicted in Figure 3, reproduced below:

FIG. 3



Programmable links 27 permit nodes N1 and N2 to be connected to either of supply lines V1 and V2. Programmable links 28 permit nodes N3 and N4 to be connected to either of ground lines G1 and G2. Ground line G1 and supply line V1 are always set at ground (0 volts) and Vcc, respectively (col. 5, l. 66 to col. 6, l. 5). However, ground line G2 and supply line V2 each can be set to ground or Vcc (*id.*).

The programmable units depicted in Figure 3 can be configured to form four different types (A-D) of memory cells. In the type A cell shown in Figure 4 (not reproduced below), the programmable units connect inverter nodes N1-N4 to only lines V1 and G1, thereby permitting the cell to function only as a RAM cell (col. 7, ll. 1-13).

In each of the type B, C, and D cells, the programmable units are configured to connect nodes N1-N4 to lines G1 and V1 and to one or both of lines G2 and V2. Each of these cells can be operated either as a RAM cell, a ROM cell storing a "1," or a ROM cell storing a "0," depending on the voltages on lines G2 and V2. Specifically, in the two type B cells shown in Figures 5A and 5B, inverter nodes N1-N4 are connected to lines G1, G2, and V1 but not to line V2, with the two cells differing in how nodes N3 and N4 are connected to lines G1 and G2.

FIG. 5A

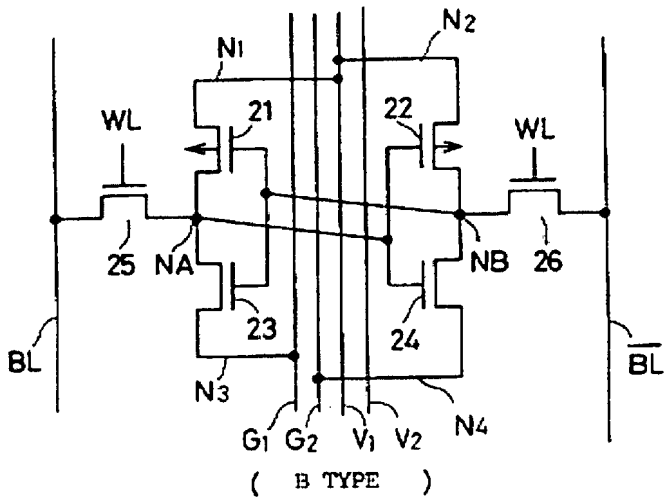
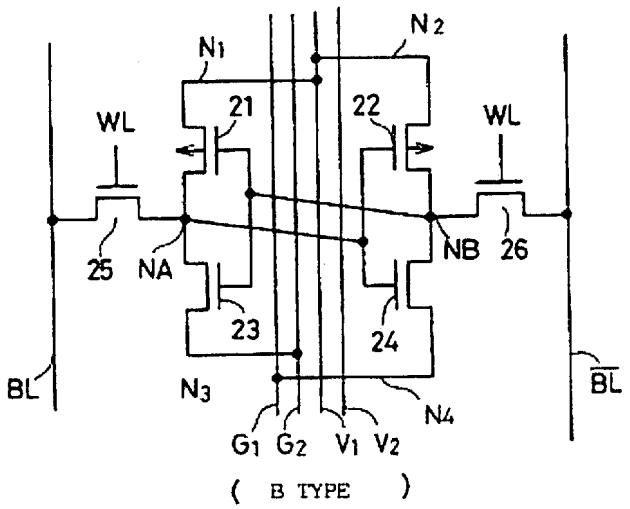


FIG.5B



Setting G2 Low (ground) in either cell causes it to function as a RAM cell (col. 7, ll. 20-22). Setting G2 high (Vcc) in the Figure 5A cell causes it to function as a ROM cell that stores a "0" (col. 7, ll. 53-56). Setting G2 high in the Figure 5B cell causes it to function as a ROM that stores a "1" (col. 7, ll. 57-59).

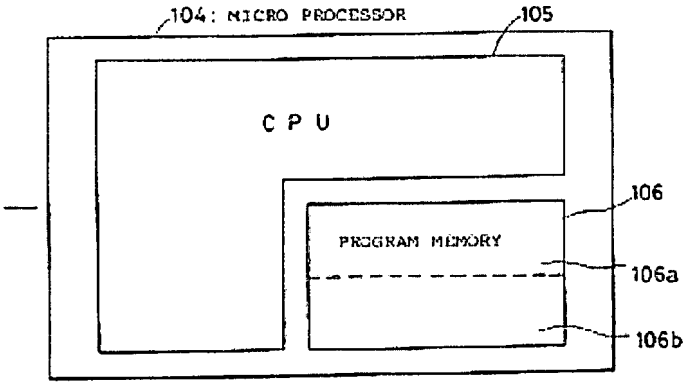
In the type C cells depicted in Figures 6A and 6B, nodes N1-N4 are connected to lines G1, V1, and V2 but not line G2. The voltage on line V2 determines whether the cell functions as a RAM cell, a ROM cell storing a "1," or a ROM cell storing a "0" (col. 7, ll. 66-68; col. 8, ll. 30-36).

In each of the type D cells depicted in Figures 7A-7D, nodes N1-N4 are connected to all of lines G1, V1, G2, and V2 and permit a cell to operate

like any one of the type B and C class cells depicted in Figures 5A, 5B, 6A, and 6B (col. 8, l. 38 to col. 9, line 7).

Figure 15, reproduced below, shows a microprocessor 104 that includes a CPU 105 and a program memory 106 (col. 11, ll. 3-17).

FIG.15



Region 106b of the memory can be used by a manufacturer as a ROM for storing a test program or a particular application program and a user can thereafter use region 106b as a RAM (*id.*). As discussed above, the ability to operate a given cell as either a ROM or a RAM is determined by configuring programmable units 27 and 28 as shown in any of the figures depicting cell types B-D, with the desired mode of operation (i.e., RAM cell, ROM cell storing a "0," ROM cell storing a "1") being selected by applying the appropriate voltage to line G2 and/or V2 (e.g., line G2 in a type B cell).

Appellants do not deny that claim 1 reads on Matsumura's Figure 3 embodiment in the manner indicated by the Examiner (Answer 3). The Examiner reads the recited first inverter on transistors 21 and 23 and the

recited second inverter on transistors 22 and 24. Although Appellants do not question the Examiner's reading of the recited I/O lines on the bit lines (BL and $\overline{BL}$), we are reading the I/O lines on lines connected to Matsumura's inverter outputs for the same reason we have held that the I/O lines read on lines connected to the inverter outputs in Appellants' Figure 3 embodiment. The Examiner reads the recited biasing circuit on lines G1, G2, V1, and V2 and, presumably, also on programmable connects 27 and 28. The requirement of the claim that the biasing circuit "forc[e] at least one of the first and second I/O lines to a known logic state when power is applied to said SRAM device" is satisfied because the voltages on G2 and V2 that cause a cell to function as a ROM cell storing a "1" or a "0" appear to be present throughout the entire time period that power is being applied to the cell (e.g., while in use by a manufacturer or a user). That is, we do not construe "when power is applied" to mean only while power is initially being applied. Nor do Appellants urge such an interpretation.

Dependent Claim 10 specifies that the "biasing circuit" of claim 1 "comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device." The Examiner does not contend that Matsumura discloses such a grounding circuit. Instead, the Examiner (Answer 9) relies for such a teaching on Shimazu, which discloses semiconductor memory devices having "a setting or resetting initialization function" (col. 1, ll. 9-10).

Shimazu's "Prior Art" Figures 1 and 2, reproduced below, each show a semiconductor memory device in the form of a "ratio latch" 4 that includes inverters 2 and 3 (col. 1, ll. 14-16).

FIG.1 PRIOR ART

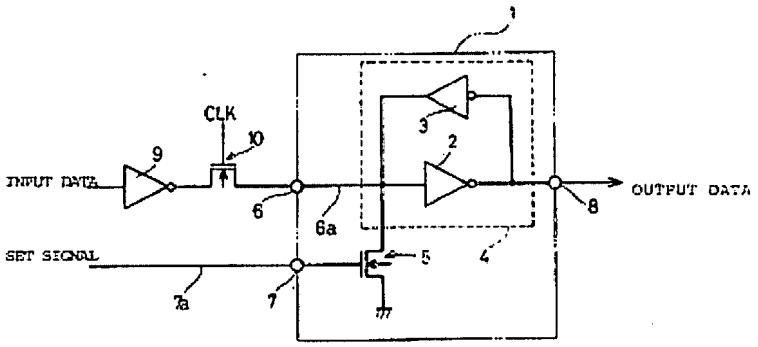
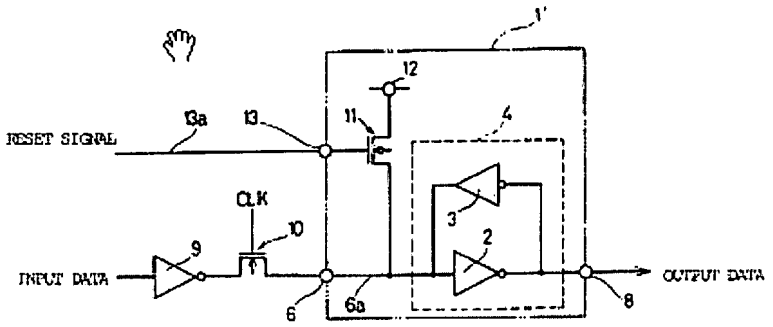


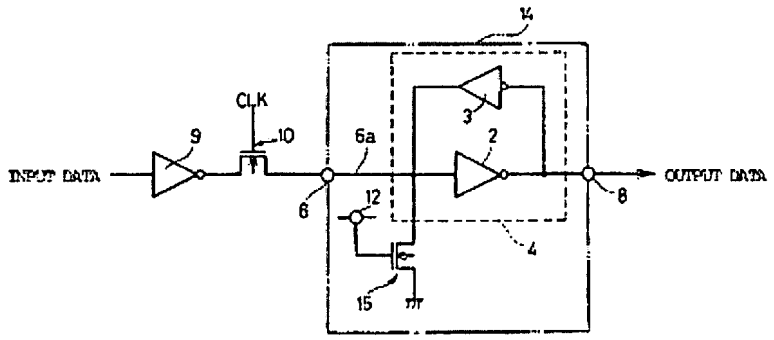
FIG.2 PRIOR ART



Transistor 5 (Fig. 1) and transistor 11 (Fig. 2) are responsive via terminals 7 and 13 to "set" and "reset" initialization signals, respectively, for setting or resetting the latches (col. 1, ll. 25-26 and 63-65). Although Shimazu does not discuss the timing or duration of these signals, it is evident from their initialization function that they are temporary signals applied after power is initially applied to the memory device.

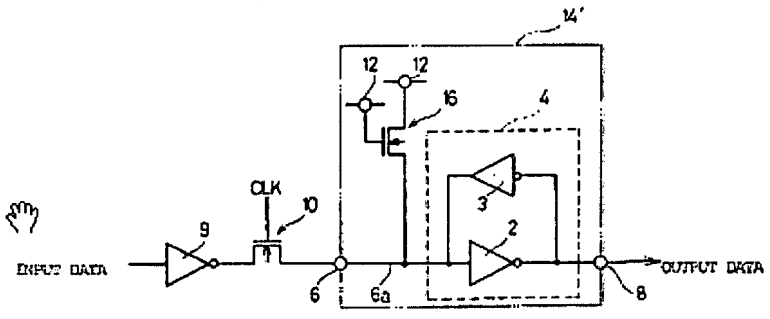
Shimazu's invention is depicted in Figures 3 and 4 (reproduced below), on which the Examiner relies. The latches shown in these figures do not require a signal line or a terminal for the exclusive use of setting or resetting the latch (col. 2, ll. 28-31). In Figure 3, transistor 15 short-circuits the data input line 6a (the output of inverter 3) to ground, thereby setting the latch, whenever the power source voltage is made higher than usual (col. 3, ll. 60-64).

FIG.3



In Figure 4, transistor 16 short-circuits the input data line 6a to the power source voltage, thereby resetting the latch, whenever the power source voltage is made higher than usual (col. 4, ll. 37-41).

FIG.4



It is evident from the fact that transistors 15 and 16 perform an initialization function that the supply voltage is increased above its usual voltage only temporarily and after power is initially applied to the memory device. The Examiner is therefore correct to find that Shimazu discloses temporarily enabling transistor 15 after power is applied to the memory cell (Answer 8). Appellants are therefore incorrect to deny that Shimazu discloses or suggests "temporarily enabling the transistor 15 after power is applied to the memory" (Br. 14).

The Examiner does not characterize Shimazu's transistor 15 (Fig. 3) as a grounding circuit. Instead, the Examiner characterizes that transistor as a programmable connect and characterizes the source of ground potential to which the transistor is connected as a grounding circuit (Final Office Action 8). Appellants deny that transistor 15 is a programmable connect, noting that it is "*fixedly* coupled to the output of the inverter 3 at one node and to ground at another" (Br. 13). Because the rejection is based on the combined teachings of the references, we are deferring consideration of this argument until after we have addressed the propriety of combining the reference teachings in the manner proposed by the Examiner.

After characterizing Shimazu's transistor 15 as a programmable connect, the Examiner held that "[i]t would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Matsumura et al. to include said biasing circuit" (Final Office Action 6) because such a biasing circuit "would allow the device to be set or

reset (See Shimazu et al., column 1, lines 7-10)" (*id.* at 7). The Final Office Action fails to explain exactly how Matsumura is to be modified. Appellants argue that the Examiner had failed to establish any motivation for combining the reference teachings in the proposed manner (Br. 14, para. 3) because

> while the Matsumura reference teaches using supply lines so as to configure a memory cell to function in a certain manner, the Shimazu reference teaches the avoidance of such supply lines. Accordingly, the combination of the Matsumura and Shimazu references as proposed by the Final Rejection relies on the irreconcilable teachings of the use of such supply lines as taught by the Matsumura reference and the elimination of such lines as taught by the Shimazu reference.

(Br. 15, para 3.)

The Examiner responded with a detailed explanation (reproduced below) of how and why it would have been obvious to modify Matsumura in view of Shimazu. For the following reasons, this explanation fails to satisfy the requirement of *KSR* and *Kahn* for "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR,* 127 S. Ct. at 1741, 82 USPQ2d at 1396; *Kahn,* 441 F.3d at 988, 78 USPQ2d at 1336.

The Examiner's detailed explanation begins as follows:

> The Matsumura et al. reference . . . disclose[s] a SRAM device that is initialized in a manner that the memory device contains a predetermined program after the initialization procedure is completed. The Matsumura et al. reference does this by supplying different voltages to the cell based on the state that the cell is desired to be in. For instance the cell disclosed in

> figure 5A is designed to be initialized into a state of "0", and the cell disclosed in figure 5B is designed to be initialized into a state of "1" simply by changing G2 to "H" or high instead of "L" or low (ground).

(Answer 8-9.)

For purposes of the following discussion, we assume the Examiner is correct to characterize Matsumura's type B, C, or D cells as being "initialized" to a state of "0" or "1." We assume the Examiner is relying on the fact that the cell can be initially used as a ROM cell (e.g., by a manufacturer) and then later used as a RAM cell (e.g., by a user).

The Examiner goes on to explain that an artisan would have been motivated to a modify Matsumura in view of Shimazu in order to reduce the number of supply lines from four (G1, G2, V1, and V2) to three:

> In order to put the cell into the different states the Matsumura et al. reference requires four supply lines that are normally set at two in the "H" or high position (V1 and V2) and two in the L or low position (G1 and G2). Depending on which of the four types of cells of the Matsumura et al. reference are being initialized, voltages on the various lines must be either switched from high to low or from low to high. This requires a switch for each of these voltage lines. Also when a voltage line is switched, only some of the cells will be initialized by the switch. For instance a change of voltage on V2 in figures 5A and 5B is not going to change the states of these cells at all. By changing the set device of Matsumura et al. from four voltage lines to the devices show[n] in figures 3 and 4 reference numbers 12, 15, and 16 of the Shimazu et al. reference, the Matsumura et al. reference would only require three power lines[,] one that is always high (V1 of Matsumura et al.), one that is always low

> (G1 of Matsumura et al.), and one that switches (12 of Shimazu et al.). If a "0" is desired to be set on BL in the Matsumura et al. reference (6 in Shimazu et al.), the device of figure 3 [of Shimazu et al.] would be used. If a "1" is desired to be set[,] the device of [Shimazu et al.'s] figure 4 would be used. This would initialize a program in memory similar to that of the Matsumura et al. reference, but would allow the entire SRAM device to be initialized with that program at the same time rather than only sections.

(Answer 9.)

This line of reasoning is unconvincing because it would not have been necessary to look beyond Matsumura to find a way to reduce the number of supply lines from four to three. The Examiner's finding that "[i]n order to put the cell into the different states the Matsumura et al. reference requires four supply lines" (Answer 9) is incorrect. The only cell configurations made from Matsumura's Figure 3 embodiment that require all four supply lines are the type D cells depicted in Figures 7A-7D. The type B cells (Figs. 5A-5B), which are capable of operation as a RAM cell, a ROM cell storing a "0," or a ROM cell storing a "1," employ only three supply lines, as do the type C cells depicted in Figures 6A and 6B. It therefore would have been obvious to reduce the number of supply lines from four to three simply by eliminating supply either of lines V1 and V2 and the corresponding programmable connections in Matsumura's Figure 3 embodiment.

Furthermore, it is not clear how the Examiner is proposing to modify Matsumura. The Examiners' reliance solely on Shimazu's transistor 15 as a programmable connect suggests the Examiner is proposing to eliminate

Matsumura's programming units 27 and 28 altogether and to add a transistor like Shimazu's transistor 15 or a transistor like Shimazu's transistor 16 (but not both) to each memory cell that is to be initialized to a "0" or a "1." While it is clear that the Examiner is proposing that those transistors be controlled by the voltage on the third supply line, it is not clear whether the voltage on that supply line is to be varied (a) in the same manner that the voltages on lines G2 and V2 are varied in Matsumura (e.g., to have a first value for a manufacturer and second value for a user, which the Examiner characterizes as initialization) or (b) in the manner that the power line voltage is varied in Shimazu (i.e., to have a first value for a short period after power-up and a second value thereafter, which Shimazu refers to as initialization). If the former type of control is intended, how does that type of control satisfy the requirement of claim 10 for temporarily enabling the grounding circuit after power is applied to the SRAM device? If the latter type of control is intended, why would the artisan have replaced Matsumura's type of initialization (assuming that term is appropriate as applied to Matsumura) with Shimazu's type of initialization?

The rejection of claim 10 is therefore reversed, as is the rejection of claim 20, which is based on the same reasoning. It is therefore not necessary to address Appellants' argument that the term "programmable connect" does not read on Shimazu's transistor 15.

DECISION

The rejection of claims 10 and 20 under 35 U.S.C. § 103(a) for obviousness over Matsumura in view of Shimazu is reversed.

REVERSED

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